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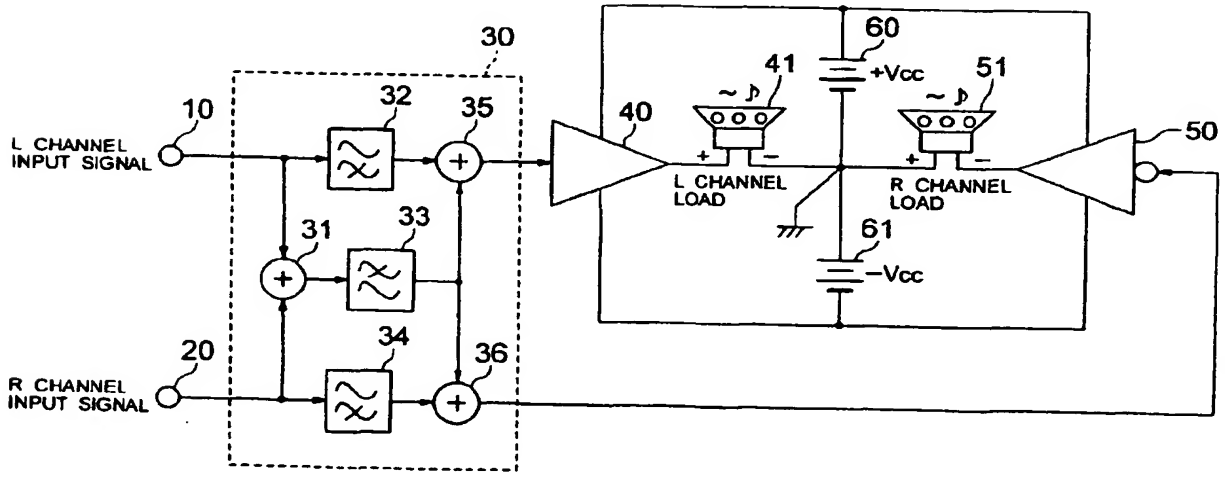
(54) D-class power amplifier with electric power regeneration function

(57) A D-class power amplifier of two channels in which an increase in power voltage due to a regenerative current is prevented and a high efficiency in utilization of electric power is attained. Two D-class power amplifying circuits (40, 50) included in the D-class power amplifier of the two channels are constructed by opposite phases. A preprocess is performed only to low frequency components of input signals (31, 33) so that they have a substantially equal amplitude in the two channels, and the resultant low frequency components are supplied to the D-class power amplifying circuits (40, 50) respectively. The other ends of loads (41, 51) connected to the D-class power amplifying circuits (40, 50) are connected to a neutral potential point of the power voltage.

FIG. 2



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OBJECTS AND SUMMARY OF THE INVENTION

[0013] The invention is made to solve the drawbacks and it is an object of the invention to provide a D-class power amplifier in which an increase in power voltage due to a regenerative current is suppressed.

[0014] According to the invention, there is provided a D-class power amplifier for supplying an amplification signal obtained by amplifying two input signals to two loads which are mutually connected at one end of each load, comprising:

two D-class power amplifying circuits having output terminals connected to the other ends of the two loads, respectively;
a preprocessing circuit for perfoming a predetermined preprocess to the two input signals and supplying the processed signals to the two D-class power amplifying circuits; and
a power supply circuit for supplying an electric power to the two D-class power amplifying circuits,

wherein one of the two D-class power amplifying circuits executes an anti-phase power amplifying process and the other of the two-D-class power amplifying circuits executes an in-phase power amplifying process,

the preprocessing circuit executes a process for equalizing amplitudes of two input signals in a low frequency band, and
a node of the two loads is connected to a potentially neutral point of an output voltage from the power supply circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015]

Fig. 1 is an explanatory diagram showing a principle of an increase in power voltage in a D-class power amplifying circuit which is driven by both of positive and negative power supplys;
Fig. 2 is a block diagram showing the construction of a D-class power amplifier according to an embodiment of the invention; and
Fig. 3 is an explanatory diagram showing the operation of D-class power amplifying circuit portions in the apparatus in Fig. 2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0016] Fig. 2 is a block diagram showing the construction of a D-class power amplifier according to an embodiment of the invention.

[0017] In Fig. 2, an L channel signal of stereophonic audio signals is supplied from an input terminal 10, while an R channel signal is likewise supplied from an input terminal 20.

[0018] A presignal processing circuit 30 is a circuit for performing a predetermined pre-signal process to those input signals and generating signals to be applied to a D-class power amplifying circuit at the post stage of the circuit. As shown in Fig. 2, the circuit comprises: high pass filters (hereinafter, simply abbreviated to HPF) 32 and 34 having a same cut-off frequency; a low pass filter (hereinafter, simply abbreviated to LPF) 33; and signal adding circuits 31, 35, and 36.

[0019] Each of those filters may be constituted by an analog filter, such as the so called LC filter an active filter and the like. It is also possible to realize the filter as a digital filter by a signal processing using what is called a digital processor (hereinafter, simply abbreviated to DSP). If the filter is constituted by the DSP, a DSP chip may be formed in such a way that whole pre-signal processing circuit 30 that additionally includes the signal adding circuits is constructed in the DSP chip.

[0020] Although D-class power amplifying circuits 40 and 50 are D-class power amplifying circuits for the L channel and the R channel, respectively, and have the same amplifying function, phases of output signals of those circuits are opposite. Each of the D-class power amplifying circuits 40 and 50 includes a low pass filter to remove a D-class switching signal and its harmonic components at an output stage thereof.

[0021] Speakers 41 and 51 are loads of the D-class power amplifying circuits 40 and 50, and convert electric signals from the L channel and the R channel into acoustic signals to be output, respectively. As mentioned above, the phase of the output signal of the D-class power amplifying circuit 40 for the L channel and that of the D-class power amplifying circuit 50 for the R channel are opposite. Therefore, the speaker 41 for the L channel and the speaker 51 for the R channel are connected to the D-class power amplifying circuits in such a way that polarities of the speakers are opposite as shown in Fig. 2, so that the reversed phase relation does not exists in the reproduced sounds in the form of acoustic signals. That is, the connection of the speakers is such that when signals of the same polarity are applied from the D-class power amplifying circuits, directions of movements of the diaphragms of the speakers are opposite to each other.

[0022] A positive side power supply 60 and a negative side power supply 61 are power supply circuits for supplying an electric power for allowing the D-class power amplifying circuits 40 and 50 to drive the speakers 41 and 51 as loads, respectively. As those power supplys, it is possible to use power supplys of a generally used type that rectifies a step-down AC output from a transformer to obtain a DC current, or power supplys of the so called switching power suplly having a high power efficiency.

[0023] With regard to the embodiment shown in Fig. 2, the operation in the presignal processing circuit 30 will be described first.

frequency band described above, magnitudes of the load currents iL1 and iL2 are substantially equal. Since the D-class power amplifying circuits 40 and 50 operate at the opposite phases, the phases of iL1 and iL2 are also opposite. In the circuits of Fig. 3, therefore, with respect to the signals of the frequency band of frequencies near about 70Hz or lower, magnitude of the consumption current i1 of the positive side power supply and that of the consumption current i4 of the negative side power supply are substantially equal. The current i4 is stopped for a period of time during which the current i1 flows. The current i1 is stopped for a period of time during which the current i4 flows.

[0037] As described in Fig. 1, the timings when the consumption currents and the regenerative currents to/from both of the positive and negative power supplys are determined by switching timings in a combination of the switching devices S1 and S2 or S3 and S4. That is, when the consumption current i1 flows, the regenerative current i3 is stopped. When the consumption current i4 flows, the regenerative current i2 is stopped.

[0038] When the above-described timings at which the currents flow will now be summarized, the consumption current i1 and the regenerative current i2 flow simultaneously to the positive side power supply +Vcc, and the consumption current i4 and the regenerative current i3 flow simultaneously to the negative side power supply -Vcc. Since a value of the regenerative current is always smaller than that of the consumption current due to the law of conservation of energy, relations of i1 > i3 and i4 > i2 are always satisfied in the circuits of Fig. 3. There is a predetermined relation between the values of the consumption currents and the values of the regenerative currents. In Fig. 3, if the consumption currents are set to i1 = i4, since the constructions of the D-class power amplifying circuits of both of the R and L channels are symmetrical, the regenerative currents are also set to i2 = i3. From the above explanation, the relations of i1 > i2 and i4 > i3 are satisfied in the circuits of Fig. 3.

[0039] That is, in the circuits of Fig. 3, at the timing when the consumption current i1 and the regenerative current i2 flow simultaneously, the whole regenerative current i2 on the R channel side is consumed as a consumption current i1 on the L channel side, and no electric power is regenerated to the positive side power supply +Vcc. The capacitor C1 of the positive side power supply unit, therefore, is not charged by the regenerative current i2 and the value of the positive side power supply +Vcc does not rise.

[0040] Since the relation of i1 > i2 is satisfied as mentioned above, the consumption current which is supplied from the positive side power supply +Vcc to the load 41 is only the difference (i1 - i2) which could not be supplemented by the regenerative current i2. The consumption current from the power supply, therefore, can be remarkably reduced as compared with the conventional system such that the whole consumption current il on the L channel side is supplied from the positive side power supply +Vcc. In association with it, a small capacity and a miniaturization of the power supply unit can be also realized.

[0041] The timing when the consumption current i4 and the regenerative current i3 flow simultaneously is also specified in a manner similar to the case of i1 and i2 mentioned above. That is, the whole regenerative current i3 on the L channel side is consumed as a consumption current i4 on the R channel side, no electric power is regenerated to the negative side power supply -Vcc, and the voltage of the negative side power supply does not rise. The current which is supplied from the negative side power supply -Vcc to the load 51 is also only the difference between the consumption current i4 and the regenerative current i3, and the electric power consumption can be reduced.

[0042] According to the present invention, the selection of the timing when the consumption current and the regenerative current flow is not limited to that in the case where i1 and i2 (or i3 and i4) flow simultaneously as in the embodiment described above. It is sufficient that a ratio of the times during which i1 and i3 flow, that is, a ratio of on/off times of S1 and S2 is equal to a ratio of the times during which i2 and i4 flow, that is, a ratio of on/off times of S3 and S4.

[0043] That is, it is not always necessary that i1 and i2 (or i3 and i4) flow simultaneously. So long as time ratios of the switching operations of the two circuits are equal, any problems hardly occur since the consumption and regeneration of the electric power are executed at a high speed while a good balance is maintained between them.

[0044] In the embodiment described above, the preprocess for equalizing the amplitudes of the L channel signal and the R channel signal has been executed with respect to only the low frequency components of the input signals of both channels because it is necessary to prevent any change to the auditory sense in association with the deterioration of the channel separation.

[0045] Specifically speaking, in the embodiment, the cut-off frequencies of the HPFs and LPF included in the presignal processing circuit 30 are set to frequencies near about 70Hz. With respect to the signals in the frequency band of the frequencies near about 70Hz or lower, therefore, the amplitude equalizing process of both of the channel signals is validated, however, the process does not act effectively with respect to the signals in a frequency band of the frequencies above 70Hz.

[0046] With respect to the signals in the frequency band of the frequencies near about 70Hz or higher, therefore, the signals which are supplied to the D-class power amplifying circuits become the input signals which are inherent to both channels and, naturally, those signals have different amplitudes and phases every channel. That is, with respect to the signals in the frequency band of the frequencies near about 70Hz or higher, the amplitude relation or phase relation regard-

FIG. 1

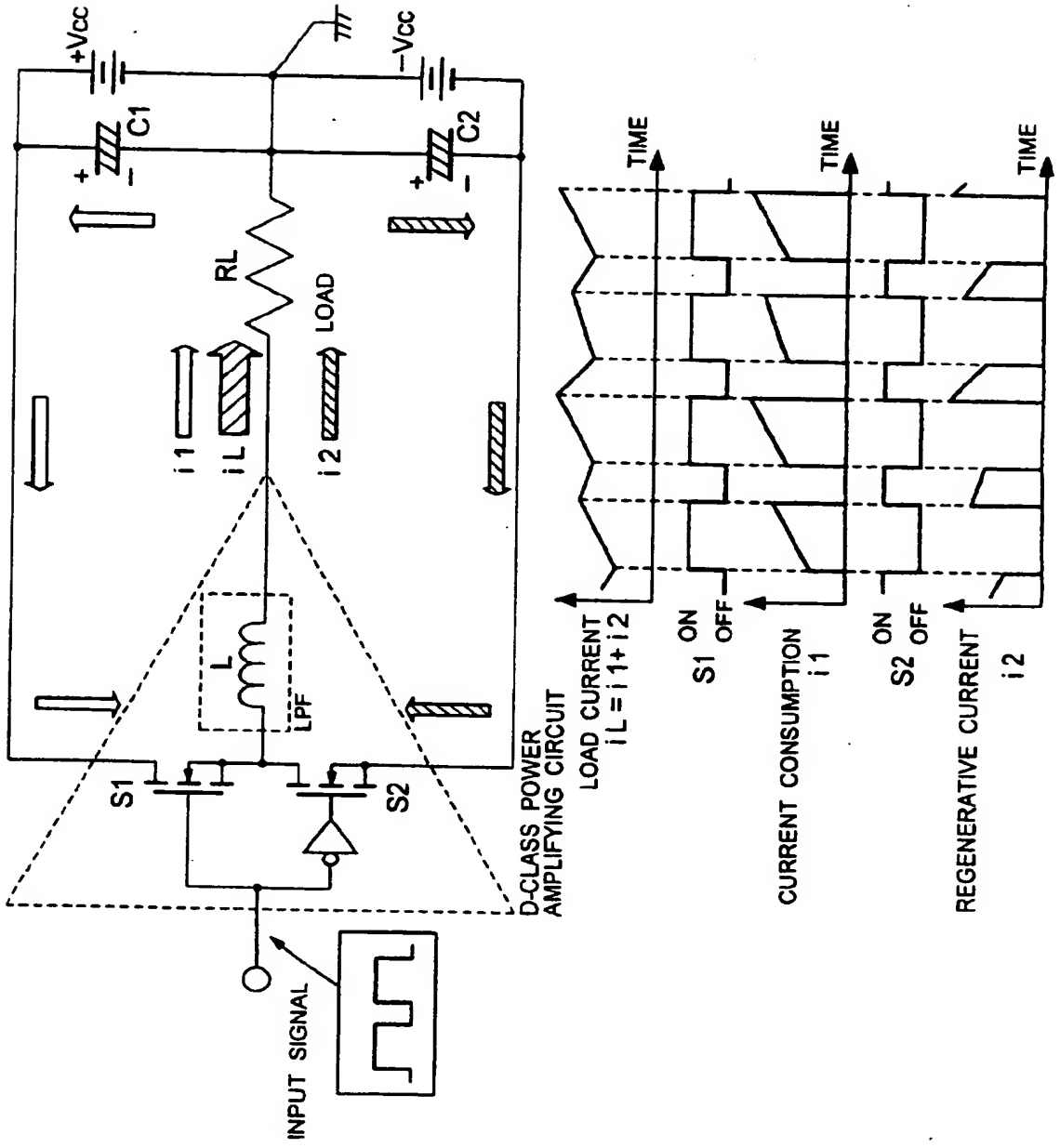
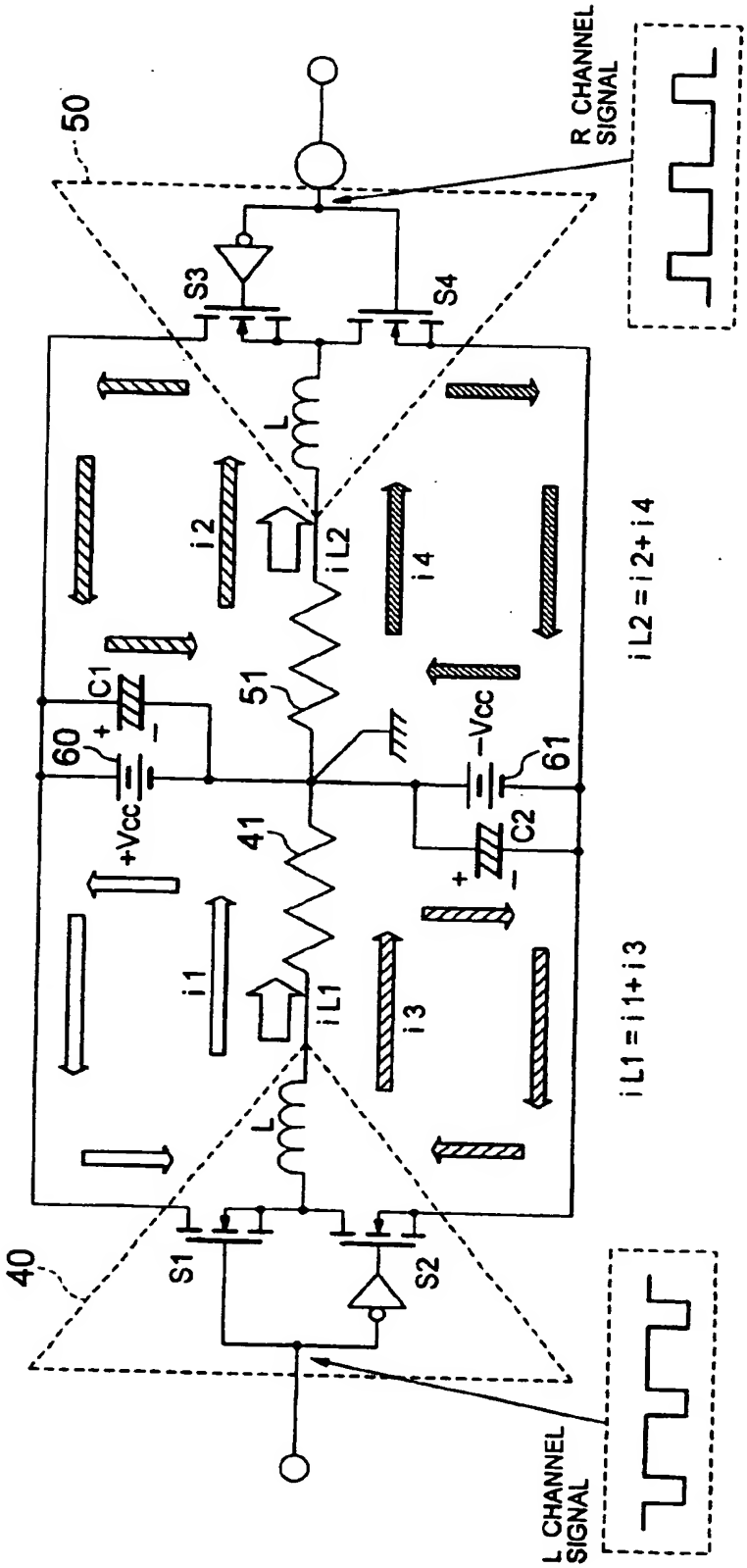

+Vcc
-Vcc
C1
C2
RL
LOAD
i1
iL
i2
L
LPF
S1
S2
INPUT SIGNAL
D-CLASS POWER AMPLIFYING CIRCUIT
LOAD CURRENT iL = i1+ i2
TIME
S1 ON OFF
CURRENT CONSUMPTION i1
S2 ON OFF
REGENERATIVE CURRENT i2

FIG. 3


50
R CHANNEL SIGNAL
S3
S4
L
i2
iL2
i4
51
C1
60
+Vcc
-Vcc
61
C2
41
i1
iL1
i3
iL2 = i2+ i4
iL1 = i1+ i3
40
S1
S2
L CHANNEL SIGNAL